	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	3	(flip with chip with interconnection) and heat$3 and press$3 and bump and (temperature same pressure same deformation)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 08:56
2	BRS	L2	104	(connect$3 with die) and heat$3 and press$3 and bump and temperature and pressure and deformation	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 08:36
3	BRS	L3	1	2 and (deformation with bump with height)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 08:38
4	BRS	L4	257	connect$3 and die and heat$3 and press$3 and bump and temperature and pressure and deformation and metal	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 08:38
5	BRS	L5	4	4 and (deformation with bump with height)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 08:55
6	BRS	L6	17	(flip with chip with interconnection) and heat$3 and press$3 and bump and (temperature same pressure same deform$5)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 09:34

	Type	L #	Hits	Search Text	DBs	Time Stamp
7	BRS	L7	0	4 and (cavity adj downward)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 09:36
8	BRS	L8	0	4 and (cavity adj upward)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 09:36
9	BRS	L9	0	(flip with chip with interconnection) and (cavity adj upward$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 09:37
10	BRS	L10	0	flip and chip and interconnection and (cavity adj upward$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 09:38
11	BRS	L11	2	flip and chip and (cavity adj upward$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 09:42
12	BRS	L12	2	flip and chip and (die with cavity with upward$3)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/11/21 09:47

L3: Entry 4 of 10 File: USPT Mar 8, 1977

DOCUMENT-IDENTIFIER: US 4010885 A
TITLE: Apparatus for accurately bonding leads to a semi-conductor die or the like

Detailed Description Text (4):
While the dimensions given herein are exemplary and can be varied according to the requirements of the industry, each inner lead within the lead frame 12 is typically 2.5 to 3 mils in width. Its length is variable. A typical length may be 100 mils. The thickness of an inner lead is typically 1.4 mils and such leads are normally made of what is described as 1 ounce copper. The ends of the leads 13 which project into the window 17 are typically plated with an intermediate layer of nickel which is 0.05 mils thick and a top layer of gold which is approximately 0.05 mils thick. The gold layer is what makes contact with the bonding pads on each die. Each bonding pad supports a small bump also made of gold when thermocompression bonding is used. Of course, metals other than gold can be used. Thermo-compression bonds to titanium-silver, silver, indium, aluminum, copper, silicon and lead are also possible. In addition to thermocompression bonding, eutectic bonding and soldering techniques may also be used. Thermocompression bonding, as the name implies, employs heat and pressure to create adhesion between the mating parts. It is a solid state bond based upon the principles of cross diffusion of the molecules; that is, there is no melting of the mating parts.

Jun 20, 1972

File: USPT

L3: Entry 6 of 10

DOCUMENT-IDENTIFIER: US 3670396 A
TITLE: METHOD OF MAKING A CIRCUIT ASSEMBLY

Brief Summary Text (6):
In the past a single headed tool called a collet has been used for bonding beam lead chips one at a time to circuit boards. The previous assembly had a rectangular collar and vacuum chuck which allowed a single chip to be picket up, registered on the circuit board and bonded by the simultaneous application of heat and pressure to the corresponding circuit board terminals. Thermocompression bonding is a type of diffusion bonding in which two metals are placed in intimate contact and pressed together while heat below the melting point of either metal is continuously applied. In the bonding operation crystals of the two metals become embedded in each other although neither metal is truly melted as in a typical welding operation.

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L3: Entry 9 of 10 File: JPAB Jul 12, 1990

PUB-NO: JP402179369A
DOCUMENT-IDENTIFIER: JP 02179369 A
TITLE: AG-OXIDE COMPOSITE CONTACT MATERIAL AND ITS MANUFACTURE

PUBN-DATE: July 12, 1990

INVENTOR-INFORMATION:

NAME	COUNTRY
NISHIJIMA, MICHIHIKO	
SHINAGAWA, RYUJI	

US-CL-CURRENT: 228/122.1
INT-CL (IPC): B23K 20/00; B32B 9/00; B32B 15/01; H01B 1/04; H01H 11/04

ABSTRACT:

PURPOSE: To reduce the quantity of consumption of a contact and the number of weldings by interposing a nonoxidized Ag alloy layer having the same component as Ag-oxide contact material as an intermediate layer between the Ag- oxide contact material and Cu (alloy).

CONSTITUTION: The nonoxidized composition Ag alloy with good jointability, namely, the Ag alloy having the same component as the Ag-oxide material is subjected to thermocompression bonding to the Ag-oxide material formed by dispersing an oxide of Cd, Sb, Sn, In, Zn, etc., in Ag. Further, the above- mentioned material is held for a prescribed time at the temperature below the melting point of both and above 400°C in a nonoxidized atmosphere of N2, etc., or an inert atmosphere to accelerate diffusion of the joined interface. The Cu (alloy) is joined to the above-mentioned material so that the Ag alloy layer is made to the intermediate layer to form composite material. By this method, the quantity of consumption of the contact point is reduced and the number of weldings is diminished to zero and the contact where peeling is also not observed at all is obtained.

DOCUMENT-IDENTIFIER: US 5821627 A
TITLE: Electronic circuit device

Detailed Description Text (187):
FIGS. 32E and 32F are views showing the concept of the second bonding steps (main connection) in the seventh embodiment of the present invention. A solid-phase diffusion reaction between the gold bumps 62 and the aluminum wiring layers 64, which is caused by thermocompression bonding, forms a reaction layer 66, electrically and mechanically connecting the gold bumps 62 to the aluminum wiring layers 64. At this time, the low-melting-point bonding metal bumps 65 exhibit two types of behaviors. One is that the low-melting-point bonding metal bumps 65 move to the side surfaces of the gold bumps due to compression bonding, as shown in FIG. 32E. The other is that the low-melting-point bonding metal bumps 65 diffuse in the gold bumps, as shown in FIG. 32F. The diffusion in the gold bumps is especially suitable for fine pitch connection because no low-melting-point bonding metal bump is confirmed in appearance. This connection is achieved by formation of the reaction layer, resulting in mechanically rigid and electrically low-resistant connection or highly reliable connection. As has been described above, the two-stage connection method such as the present invention can facilitate the repairing operation for a semiconductor device and obtain highly reliable connection.

L5: Entry 1 of 2 File: USPT Oct 31, 1995

DOCUMENT-IDENTIFIER: US 5463245 A
TITLE: Semiconductor integrated circuit device having sealing means

Brief Summary Text (5):
A semiconductor integrated circuit device such as an IC and LSI is packaged to protect the semiconductor substrate (chip) on which an integrated circuit is formed from a mechanical damage and a contamination source such as dusts, chemical, gases, and moisture. A package used for packaging the semiconductor integrated circuit device is required to have characteristics such as high hermetic sealing, high heat resistance to high temperatures applied in the assembling process, high mechanical strength, chemically stable characteristic, and good electrical properties such as high insulating property and high frequency characteristic, and resin or ceramics may be used as the material thereof. When resin is used, a DIP (Dual In-line Package) type semiconductor integrated circuit device shown in FIG. 1 may be provided, for example. The semiconductor integrated circuit device is obtained by fixedly attaching a chip 100 having a semiconductor integrated circuit formed thereon to a chip mounting portion 25 of a lead frame, for example, by use of an electrical conductive adhesive agent 35. The chip 100 includes leads 45 for connection with an external circuit, and in general, the lead 45 is formed of a lead frame. A bonding portion 55 is formed on one end of the lead 45 and a connection electrode 65 such as an Al pad formed on the chip 100 is electrically connected to the bonding portion via a bonding wire 75 formed of Al or Au, for example. The chip 100, chip mounting portion 25, bonding wire 75 and part of the lead 45 are covered with mold resin 85 by use of the transfer molding method. As an example of the document disclosing the above technique, there is provided an article "LARGE-CAPACITY MEMORY BOARD BY CHIP LAMINATION MOUNTING" of "THIRD MICROELECTRONICS SYMPOSIUM (MES '89)" July 1989 (TOKIO) in which the technique of protecting the chip surface by use of epoxy-series protection resin is disclosed.

Detailed Description Text (4):
The impurity diffusion region 3 is formed to electrically connect the semiconductor integrated circuit 39 formed in the semiconductor substrate 1 to a lead 4 used for connecting the semiconductor integrated circuit 39 to an exterior circuit. In order to connect the lead 4 to the impurity diffusion region 3, a connection electrode 5 is formed on the inactive region 12 in the peripheral portion of the semiconductor substrate 1 which is separated from the active region 11 by means of the oxide film 2 and 22 formed on the semiconductor substrate 1. The connection electrode 5 is formed on the N-type impurity diffusion region 3 which is exposed to the main surface of the semiconductor substrate 1 and is constructed by a barrier metal layer 51 formed of refractory metal such as W in direct contact with the diffusion region and an Au bump electrode 52 formed on the metal layer. The barrier metal layer 51 can be formed of not only refractory metal such as W, Mo, or Ti but also the nitride thereof such as TiN or a silicide such as Ti.sub.2 Si. For example, the lead 4 formed of Sn-plated Cu is bonded to the bump electrode 52 by thermocompression bonding. The main surface of the semiconductor substrate 1 is covered with an insulation film 61 such as an SiO.sub.2 film and the bump electrode 52 projects upwardly to a position above the insulation film 61. The oxide film 22 and the insulation film 61 may be formed at the same time. Further, a metal wiring 7 of Al or the like is formed on the insulating film 61 above the active region 11 of the semiconductor substrate 1. The metal wiring 7 is electrically connected to the semiconductor integrated circuit 39 formed in the active region 11. Then, the metal wiring 7 is electrically connected to the impurity diffusion region 3 via a contact

hole 13 formed in the insulating film 61.

Detailed Description Text (10):
Next, a plurality of contact holes 13, 14 are formed by selectively etching the inter-level insulating film 61 so as to partly expose the impurity diffusion regions 3 of the active region 11, the impurity diffusion regions 3 of the active region 11 and an area other than the impurity diffusion regions 3 of the active region 11. A barrier metal layer 51 used as a ground metal layer of the connection electrode 5 is formed in the contact hole 14 of the inactive region 12 and a bump electrode 52 of Au or the like is formed on the barrier metal layer 51. For example, A layers are formed in the contact holes 13 of the impurity diffusion region 3 of the active region 11 and selectively connected to A wirings 7 which are formed on the inter-level insulating film 61. Then, an inter-level insulating film 62 is formed on the inter-level insulating film 61 to cover the A wirings 7 formed on the active region 11. The process up to this step is effected for the silicon wafer obtained by slicing a single crystal ingot of silicon. After forming the Al wiring 7 and connection electrode 5, the silicon wafer is divided into a plurality of semiconductor substrates 1 as shown in FIG. 4.

Detailed Description Text (12):
After this, as shown in FIG. 5, one end portion of the lead 4 formed of Cu or the like is mounted on the bump electrode 52 and bonded thereto by thermocompression bonding. Since the surface of the lead 4 is Sn-plated, Sn and Au of the bump electrode 52 create eutectic to fixedly connect the lead 4 and connection electrode 5 together. After a passivation film 8 is formed on the entire surface of the semiconductor substrate 1 including the above connection portions, organic bonding agent 9 such as epoxy resin is coated on the passivation film 8 as shown in FIG. 1 and then a sealing substrate 10 formed of silicon semiconductor having no active region is formed on the bonding agent 9 to bond the semiconductor substrate 1 and the sealing substrate 10 together. As shown in FIG. 6, the front end portion of the lead 4 is mounted on a circuit board 16 by use of a heating tool 17.

Detailed Description Text (13):
Next, a second embodiment is explained with reference to FIG. 7, FIG. 8 and FIG. 9. FIG. 7, FIG. 8 and FIG. 9 are partial cross sectional views for illustrating the process for manufacturing the semiconductor integrated circuit device. As shown in FIG. 7, this embodiment is the same as the former embodiment in the process up to the step of forming the contact holes 13, 14 in the inter-level insulating film 61 on the semiconductor substrate 1. In this embodiment, instead of the barrier metal layer 51 used in the former embodiment, an A layer 53 is deposited as the ground metal layer in the contact hole 14 formed in the inactive region 12 in the step of forming the Al wiring 7 on the active region 11 and an Au bump 52 is formed on the Al layer 52 as shown in FIG. 8. An Au-Ge bump may be used instead of the Au bump. Since the lead 4 is formed of Sn-plated Cu, an Au--Sn eutectic is formed between the lead 4 and the bump 52 to fixedly connect them together. After this, as shown in FIG. 9, a passivation film 8 such as a BPSG film which is made flat is formed on the semiconductor substrate 1 including the inactive region 12 and then a sealing substrate 10 formed of a silicon semiconductor substrate is formed on the passivation film by use of epoxy resin bonding agent 9.

Detailed Description Text (15):
Next, a third embodiment is explained with reference to FIG. 10 and FIG. 11. FIG. 10 and FIG. 11 are a partial cross sectional view of the semiconductor integrated circuit device and a plan view of the semiconductor substrate. This embodiment has a feature in a sealing means for mounting the sealing substrate 10 on the semiconductor substrate 1 and utilizes a glass sealing body instead of the organic bonding agent 9 used in the former embodiment. As shown in FIG. 10, a semiconductor integrated circuit 39, wiring 7 and inter-level insulating film 61 are formed on the semiconductor substrate 1, a connection electrode 5 which is electrically connected to an impurity diffusion region 3 used as the wiring layer is formed on the inactive region 12, and a lead 4 is mounted on a bump electrode 52 of the electrode 5. A barrier metal layer 51 is formed under the bump electrode 52. After the active region 11 including the wiring 7 is covered with an inter-level insulating film 62, a passivation film 8 such as a BPSG film is formed on the lead 4 and wiring 7. The wiring 7 may be the first-layered wiring on the semiconductor substrate 1 or the

topmost wiring layer of the multi-layered wiring. A ring-form glass sealing body 91 formed of low melting glass is formed on that portion of the passivation film 8 which lies above the inactive region 12. Then, the sealing substrate 10 is mounted on the semiconductor substrate 1. For example, a metalized layer 92 of Au or the like is formed on that portion of the sealing substrate 10 which corresponds in position to the glass sealing body 91, the sealing substrate 10 is mounted on the semiconductor substrate 1 with the metalized layer 92 superimposed on the glass sealing body 91 and they are bonded together by thermocompression bonding at temperatures of approx. 200.degree. C. With the above method, the airtightness of the package can be enhanced. Further, it is possible to mount the sealing substrate 10 on the semiconductor substrate 1 without using the metalized layer 92 and attain the air-tightness only by use of the glass sealing body 91.

Detailed Description Text (17):
Next, a fourth embodiment is explained with reference to FIG. 12 and FIG. 13. FIG. 12 and FIG. 13 are a partial cross sectional view of the semiconductor integrated circuit device and a plan view of the semiconductor substrate. Like the third embodiment, this embodiment has a feature in a means for mounting the sealing substrate 10 on the semiconductor substrate 1. As shown in FIG. 12, a semiconductor integrated circuit 39, wiring 7 and inter-level insulating film 61 are formed on the semiconductor substrate 1, a connection electrode 5 which is electrically connected to an impurity diffusion region 3 used as the wiring layer is formed on the inactive region 12, and a lead 4 is mounted on a bump electrode 52 of the electrode 5. A barrier metal layer 51 is formed under the bump electrode 52. After the active region 11 including the wiring 7 is covered with an inter-level insulating film 62, a passivation film 8 such as a BPSG film is formed on the lead 4 and wiring 7. The wiring 7 may be the first-layered wiring on the semiconductor substrate 1 or the topmost wiring layer of the multi-layered wiring. As shown in FIG. 13, for example, a sealing body 93 formed of Al or the like is formed in a belt-like ring form on the inter-level insulating film 62 by the sputtering method or the like. A similar sealing body 94 of Al or the like is formed on the sealing substrate 10 by the sputtering method, for example. Then, the sealing substrate 10 is mounted on the semiconductor substrate 1 with the sealing bodies 93 and 94 superposed on each other. Then, the sealing substrate 10 is fixedly bonded to the semiconductor substrate 1 by applying ultrasonic vibration to the sealing bodies 93 and 94 to bond the sealing bodies together. With the above method, the airtightness of the package can be enhanced.

Detailed Description Text (19):
Next, a fifth embodiment is explained with reference to FIG. 14. This embodiment has a feature that the semiconductor substrate is used for the sealing substrate, the active region is formed in the semiconductor substrate, and the semiconductor integrated circuit is formed in the active region. The external appearance thereof is similar to that obtained by superposing the conventional semiconductor chips on each other, but it is different in that the external surface of the semiconductor chip, that is, the inactive region of the semiconductor substrate constitutes a package and the external connection leads are connected to the peripheral portion of the semiconductor substrate which is an inactive region. FIG. 14 is a partial cross sectional view of a semiconductor integrated circuit device. As shown in FIG. 14, a semiconductor integrated circuit 39, wiring 7 and inter-level insulating film 61 are formed on the semiconductor substrate 1, a connection electrode 5 which is electrically connected to an impurity diffusion region 3 used as the wiring layer is formed on the inactive region 12, and a lead 4 is mounted on a bump electrode 52 of the electrode 5. A barrier metal layer 51 is formed under the bump electrode 52. After the active region 11 including the wiring 7 is covered with an inter-level insulating film 62, a passivation film 8 such as a BPSG film is formed on the lead 4 and wiring 7. The wiring 7 may be the first-layered wiring on the semiconductor substrate 1 or the topmost wiring layer of the multi-layered wiring.

Detailed Description Text (20):
On the other hand, in the sealing substrate 10, a semiconductor integrated circuit, wiring 70 and inter-level insulating film 610 are formed on the active region 110, a connection electrode 50 which is electrically connected to an impurity diffusion region 30 used as the wiring layer is formed on the inactive region 120, and a lead 40 is mounted on a bump electrode 520 of the connection electrode 50. A barrier

End of Result Set

L5: Entry 2 of 2 File: USPT Mar 8, 1977

DOCUMENT-IDENTIFIER: US 4010885 A
TITLE: Apparatus for accurately bonding leads to a semi-conductor die or the like

Brief Summary Text (4):
To increase production and yield, the semi-conductor industry has commenced using film-carrier techniques in place of the more widely used wire-bonding technique. A film carrier consists of a strip of film or foil having sprocket holes at its edge which incorporates lead frame. The leads are simultaneously bonded to the bonding pads on the die by a bonder. Sprocket holes along the sides of the film carrier function to provide a means to advance the film carrier after a die has been bonded and they also serve to register the lead frame precisely over the die, ensuring that each lead is centrally located over its own pad on the die.

Detailed Description Text (1):
Referring now to the drawings in detail, wherein like numerals indicate like elements, there is shown in FIG. 8 a lead frame film-carrier 10 for preformed inner leads 12. The film-carrier 10 is per se known in the art and generally comprises a plastic (e.g., polyimide) carrier 14, resembling movie film, that has lead frames 12 mounted along its surface.

Detailed Description Text (3):
The film 14 is presently made of polyimide which is a thermosetting-type plastic characterized by its ability to withstand high temperatures and by its dimensional stability. The lead frames 12 are made of a metal foil (e.g., copper, nickel, gold or a combination of them) which is bonded to the film 14 and etched to form the leads by a process not relevant to the description of the present invention. The inner end 13 of each of the leads projects over a window 17 in the film 14 and by means of the bonding apparatus herein described they are aligned with the bonding pads on each die and thereafter gang-bonded, (as by thermocompression bonding), to the bonding pads. (As used throughout this disclosure and the claims, the term "die" refers to a semi-conductor device such as, by way of example, an integrated circuit. The term "chip" and "die" are often used interchangeably in the industry and are so used in this disclosure.) Film-carriers were developed to provide for gang-bonding as a faster and more reliable method of providing the conductive leads than the well-known wire-bonding technique. The gang-bonding process allows each lead frame on the film 14 to be attached to a die in a single stroke of the bonding tool. The operation releases the die from the matrix in which it is held and the bonded dies are reeled onto a take-up spool. Thereafter, they are attached to outer lead frames or encapsulated in integrated circuit packages.

Detailed Description Text (4):
While the dimensions given herein are exemplary and can be varied according to the requirements of the industry, each inner lead within the lead frame 12 is typically 2.5 to 3 mils in width. Its length is variable. A typical length may be 100 mils. The thickness of an inner lead is typically 1.4 mils and such leads are normally made of what is described as 1 ounce copper. The ends of the leads 13 which project into the window 17 are typically plated with an intermediate layer of nickel which is 0.05 mils thick and a top layer of gold which is approximately 0.05 mils thick. The gold layer is what makes contact with the bonding pads on each die. Each bonding pad supports a small bump also made of gold when thermocompression bonding is used. Of course, metals other than gold can be used. Thermo-compression bonds to